65 nm Press Release
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Intel's 65 nm Logic Technology

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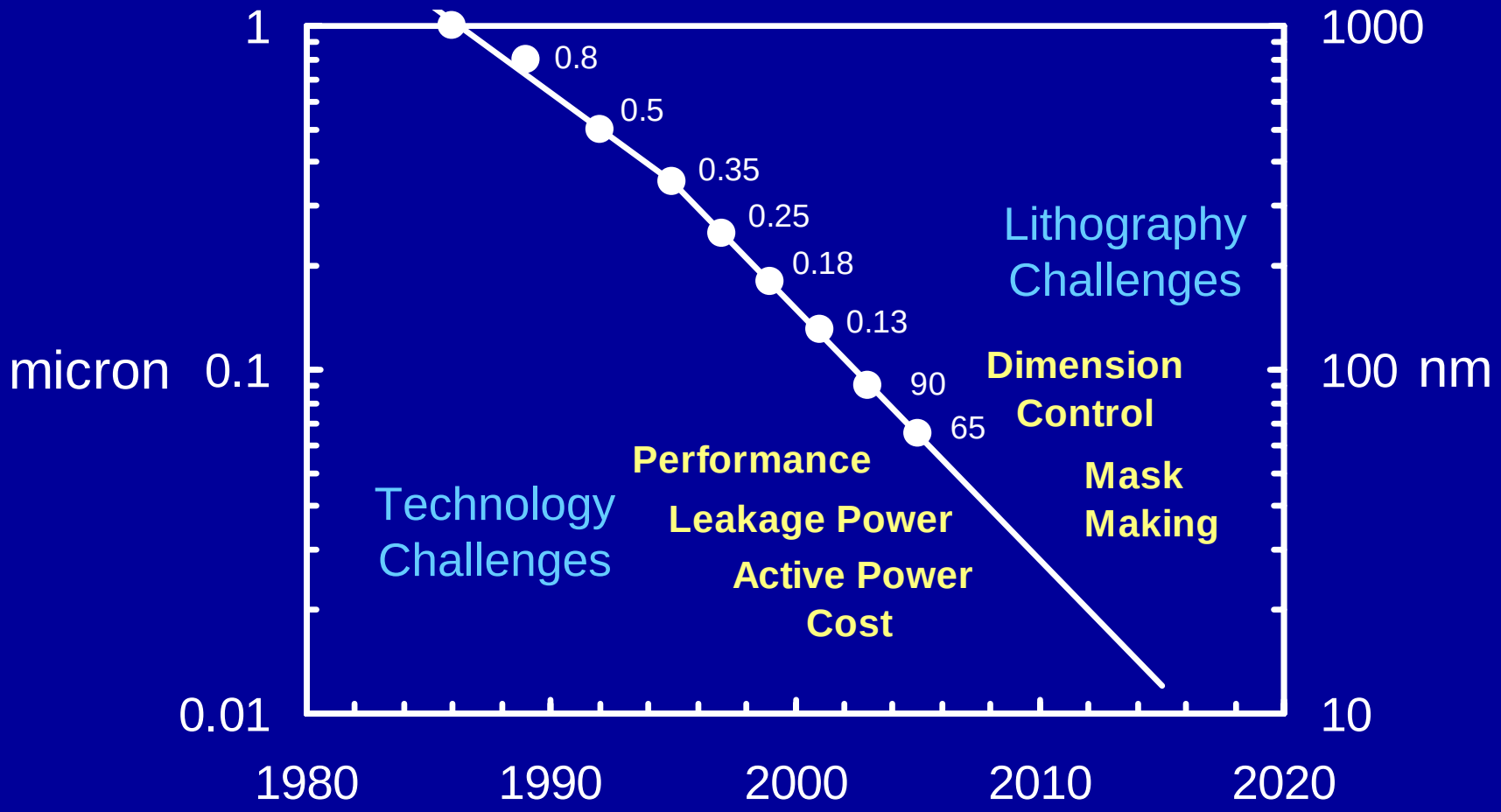
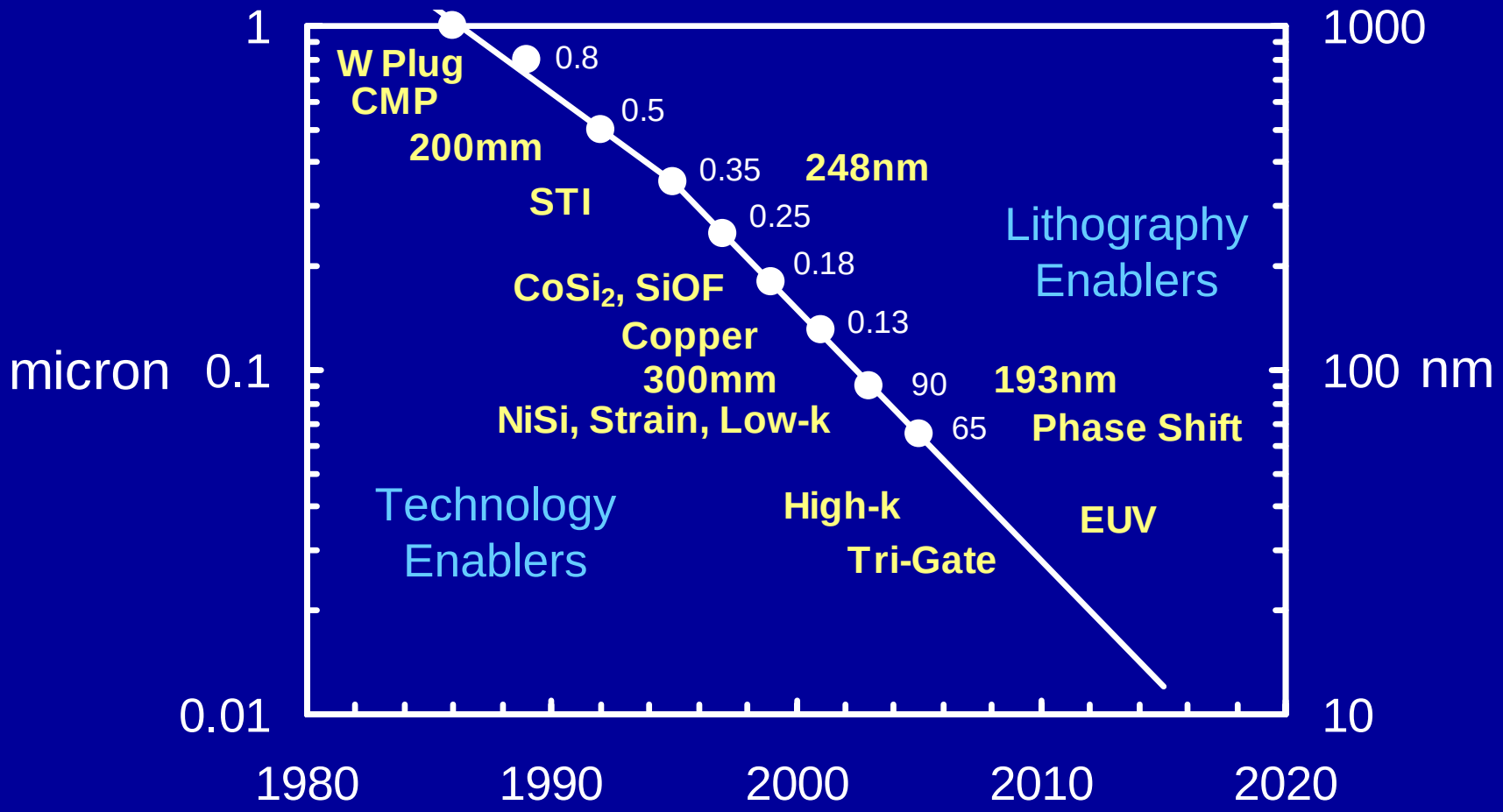
Scaling Gets Tougher at Smaller Dimensions



Scaling Gets Tougher at Smaller Dimensions



Intel continues to develop and implement new materials and structures to meet the challenge

What are We Announcing Today?

- Intel is disclosing details of its 65 nm generation logic technology which provides improved performance and reduced power:
  - 1.2 nm transistor gate oxide
  - 35 nm transistor gate length
  - Enhanced strained silicon technology
  - 8 layers of copper interconnect
  - Low-k dielectric
- This technology is being demonstrated on fully functional 70 Mbit SRAM chips with >0.5 billion transistors
- Intel's 65 nm technology is on track for delivery in 2005

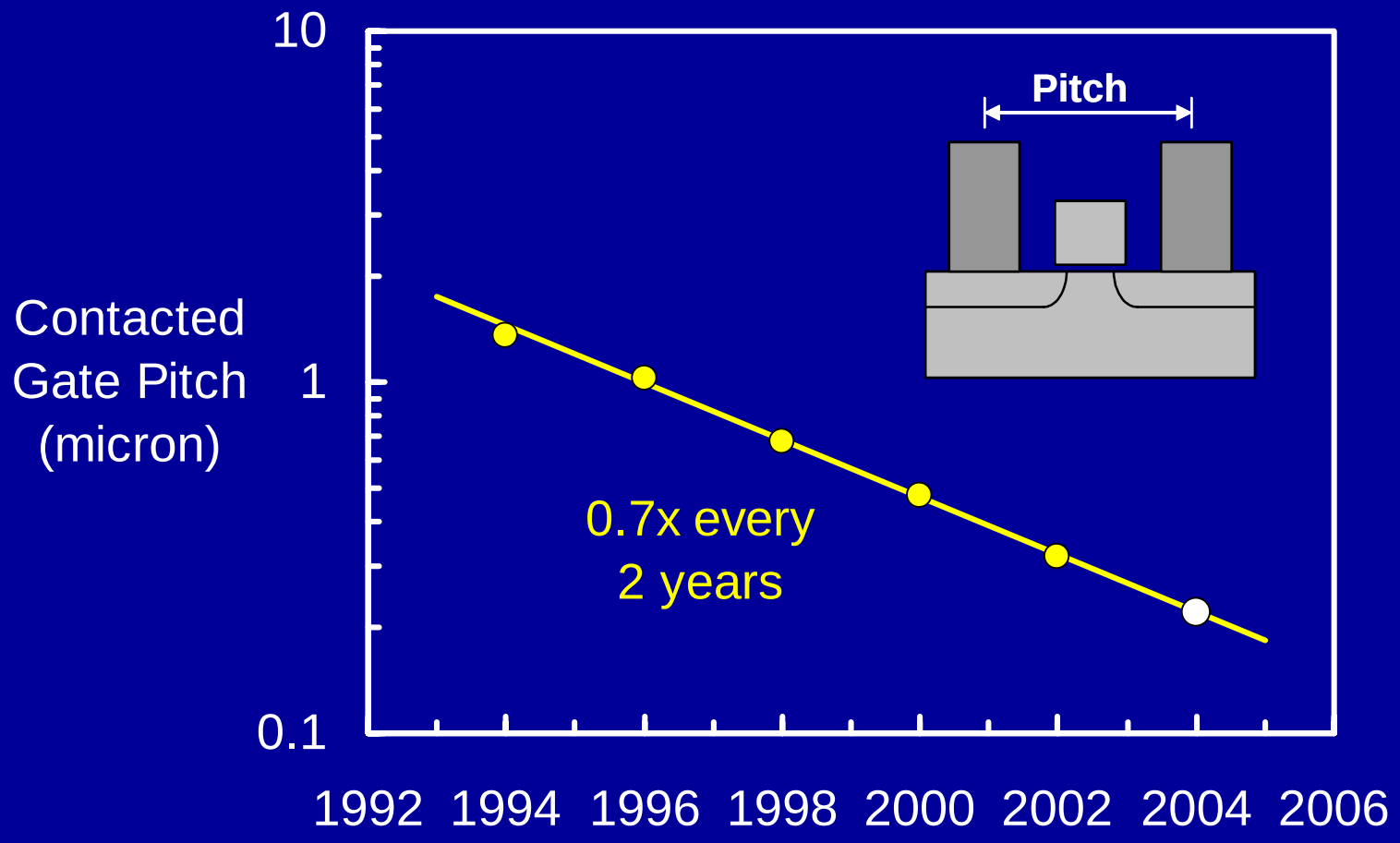
Intel's Logic Technology Evolution

Process Name	Px60	P1262	P1264	P1266	P1268
Lithography	130nm	90nm	65nm	45nm	32nm
Gate Length	70nm	50nm	35nm	25nm	18nm
Wafer (mm)	200/300	300	300	300	300
1st Production	2001	2003	2005	2007	2009

Moore's Law continues!

Intel continues to introduce a new technology generation every 2 years

Key Density Indicator Continues to Scale



Transistor gate pitch continues to scale 0.7x per generation

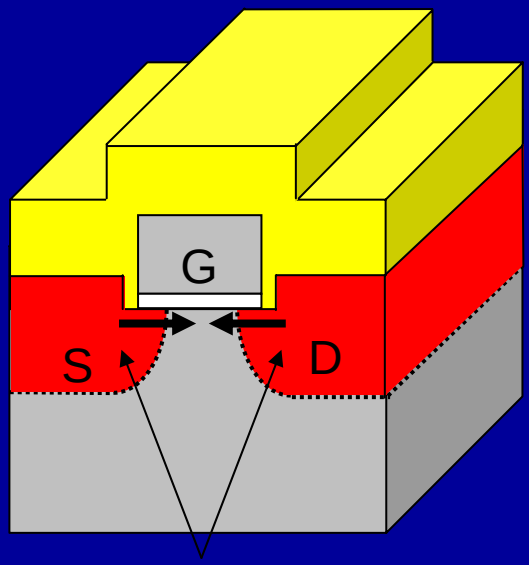
0.7x linear scaling provides 2x transistor density improvement

65 nm Generation Transistors

- 1.2 nm gate oxide, 35 nm gate length for improved performance
- 220 nm contacted gate pitch for improved density
- NiSi for low resistance cap on gates and source-drains
- Intel's unique uniaxial strained silicon technology, first introduced on the 90 nm generation, is further enhanced on 65 nm transistors for improved performance
- At the 65 nm generation, strained silicon improves performance ~30% relative to non-strain

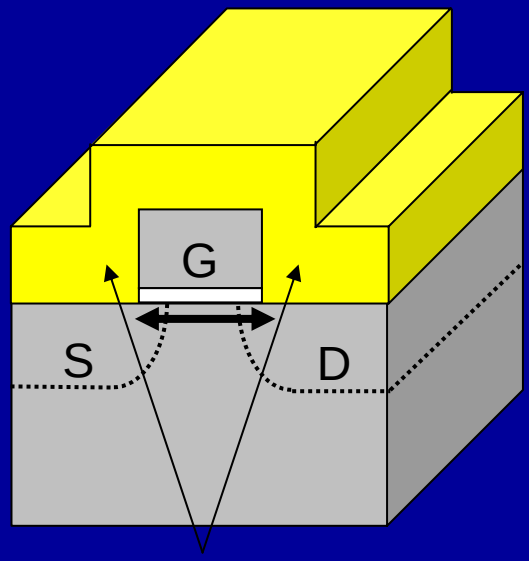
Intel has developed a second generation of strained silicon technology while others are still struggling to develop their first generation

Intel's Strained Silicon Technology



Selective SiGe S-D

PMOS
Uniaxial Compressive Strain

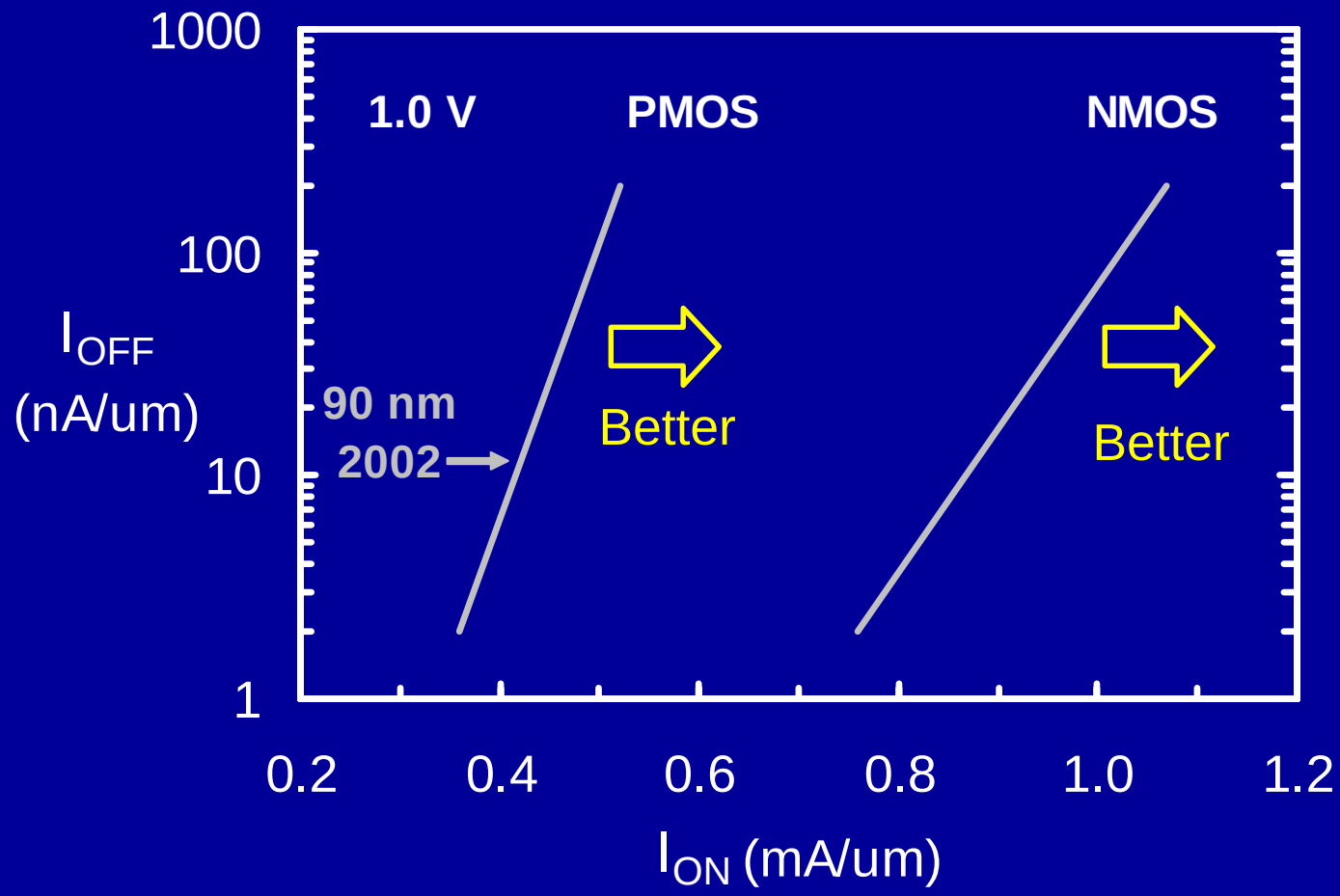


Tensile Si_3N_4 Cap

NMOS
Uniaxial Tensile Strain

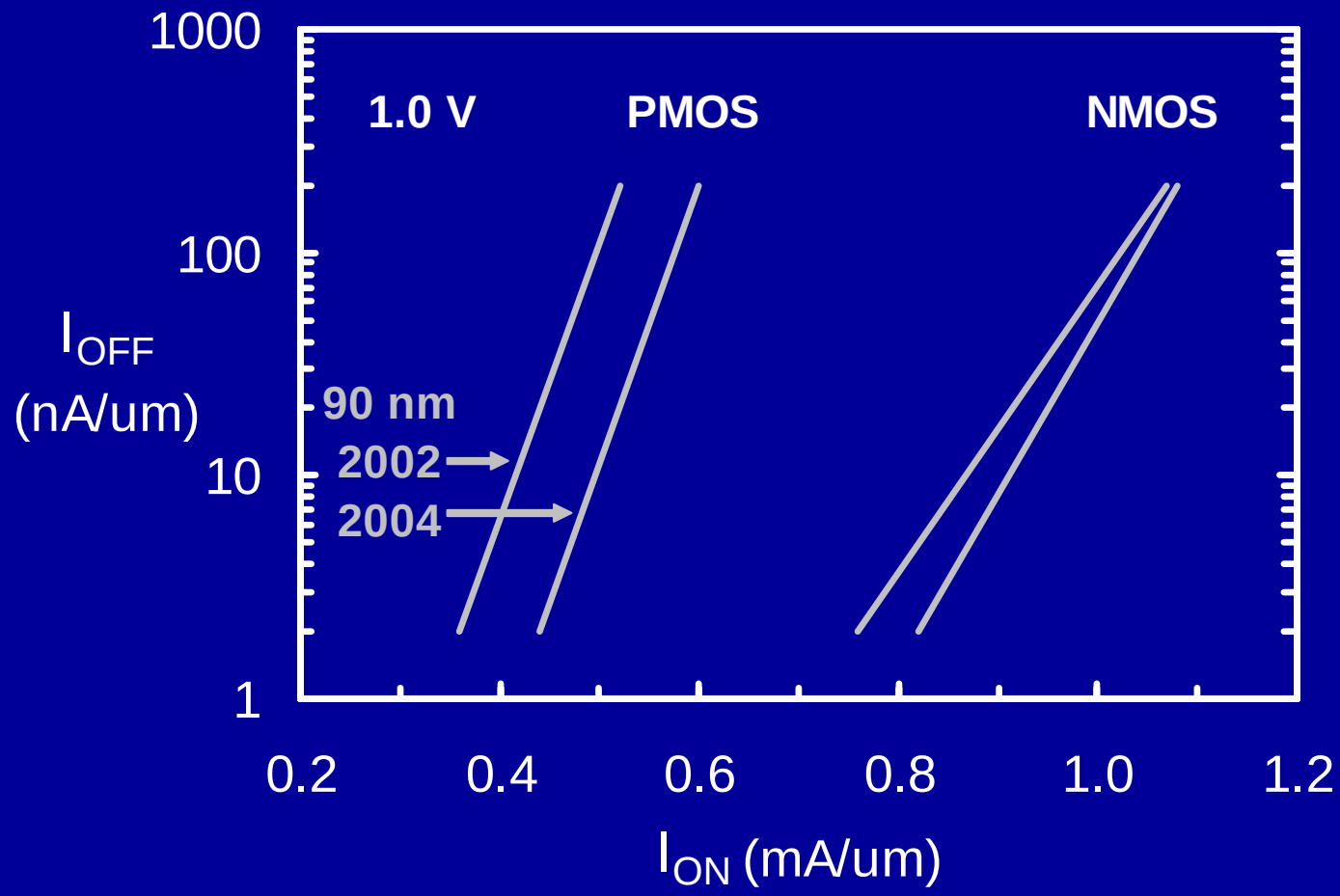
From Intel's 90 nm press release, October 2003

Improved Transistor Performance



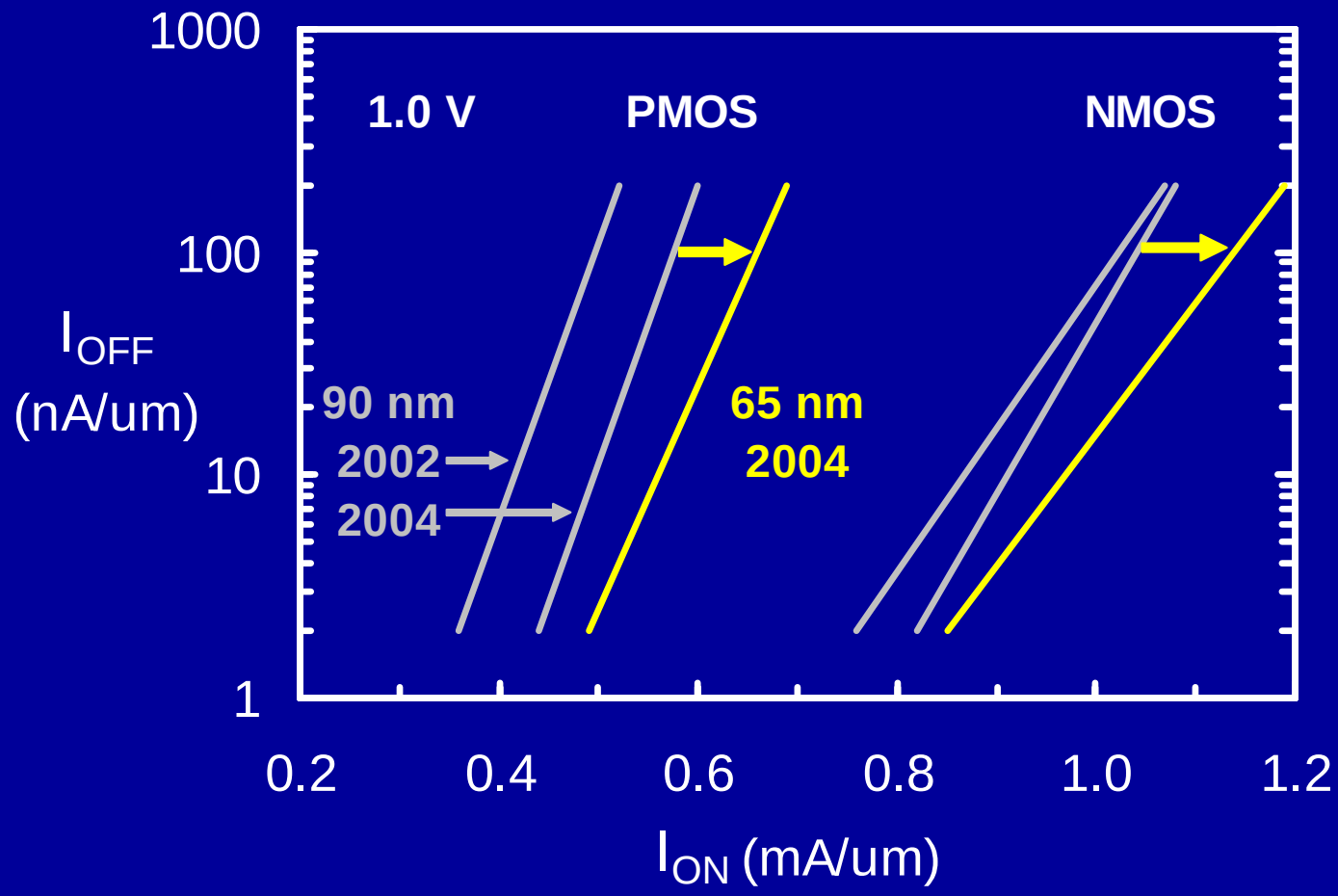
Improved transistors provide increased drive current (I_{ON}) at constant leakage current (I_{OFF})

Improved Transistor Performance



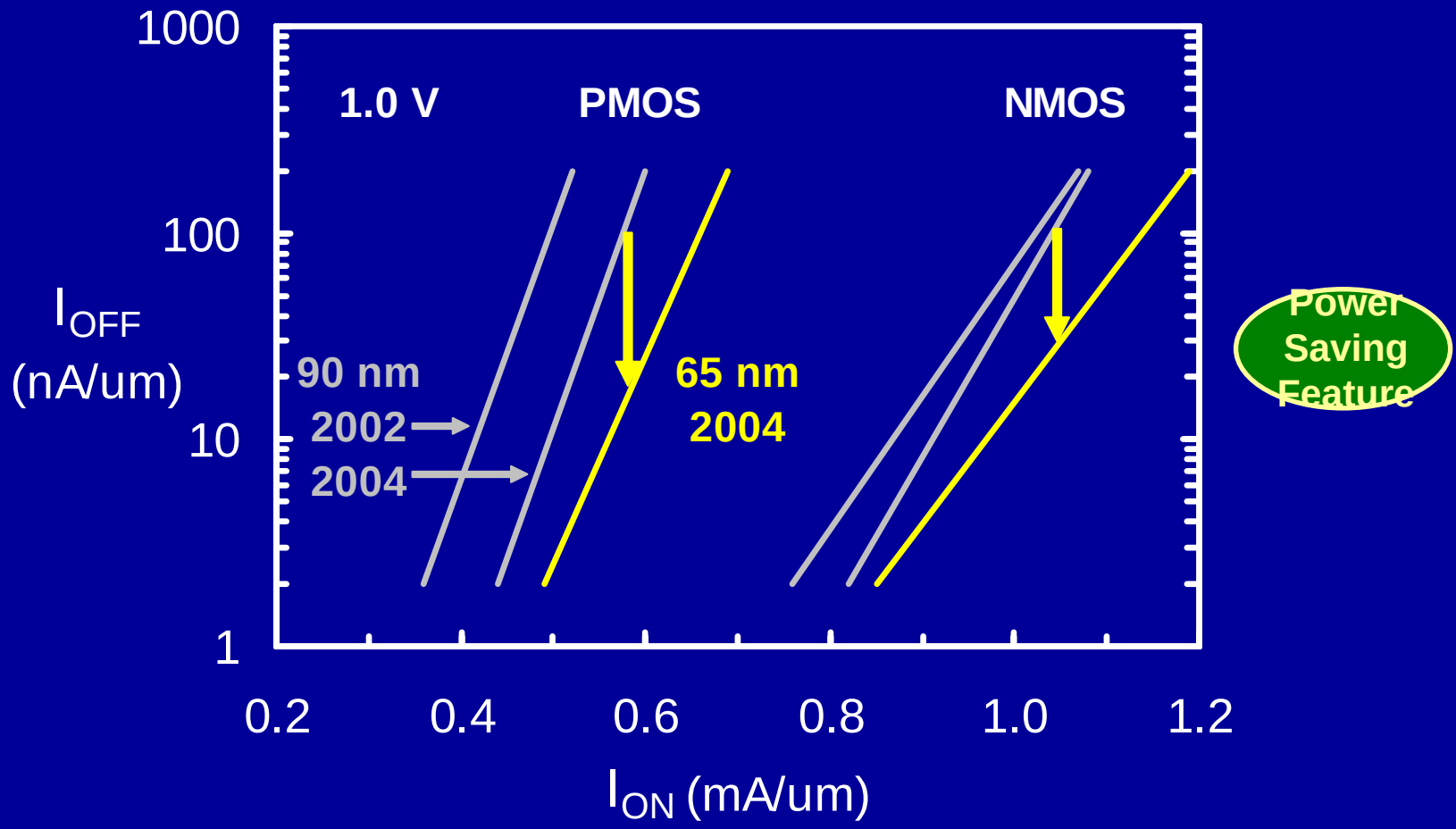
90 nm transistors have continued to improve

Improved Transistor Performance



65 nm transistors increase drive current 10-15% with enhanced strain

Improved Transistor Performance

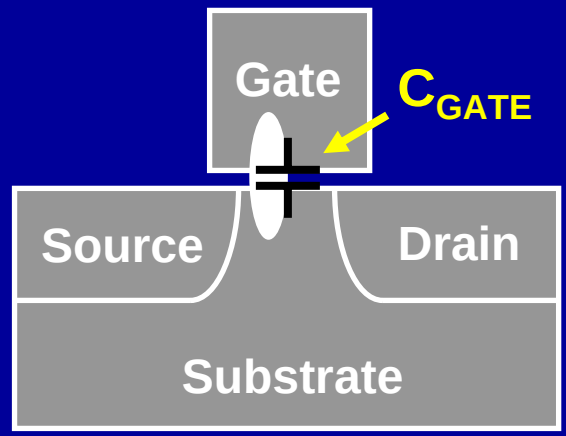


65 nm transistors can alternatively provide ~4x leakage reduction

No other company has matched these performance-leakage capabilities

Reduced Gate Capacitance

- Gate oxide thickness is held constant at 1.2 nm to avoid increased gate leakage
- Gate capacitance (C_{GATE}) reduced ~20% due to smaller gate length (35 nm)
- Lower gate capacitance reduces chip active power
- Combination of higher drive current and lower gate capacitance provides ~1.4x increase in switching frequency

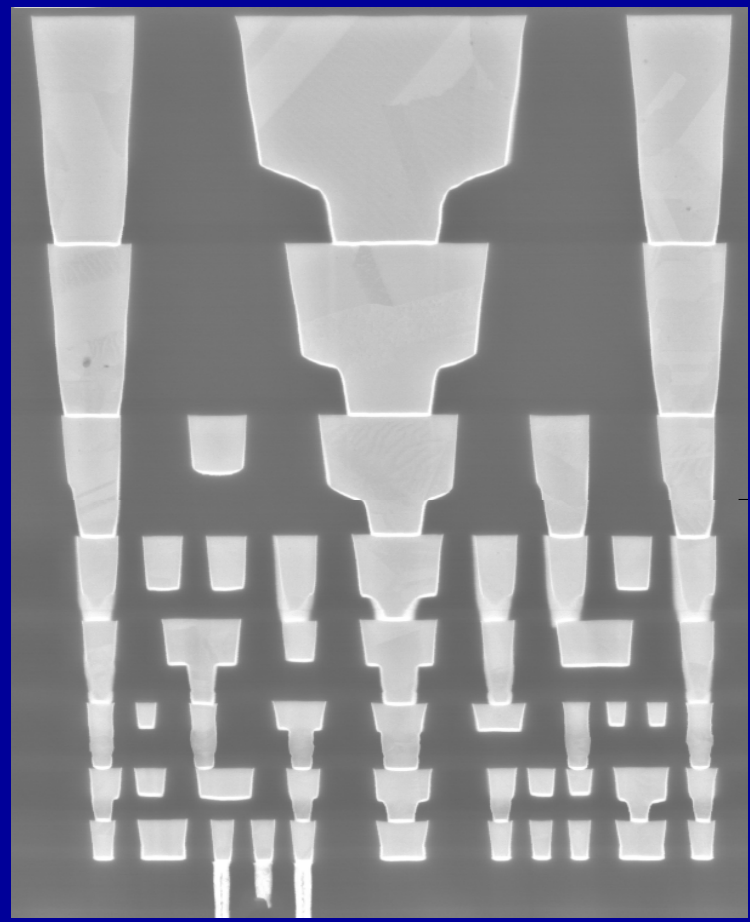


Power Saving Feature

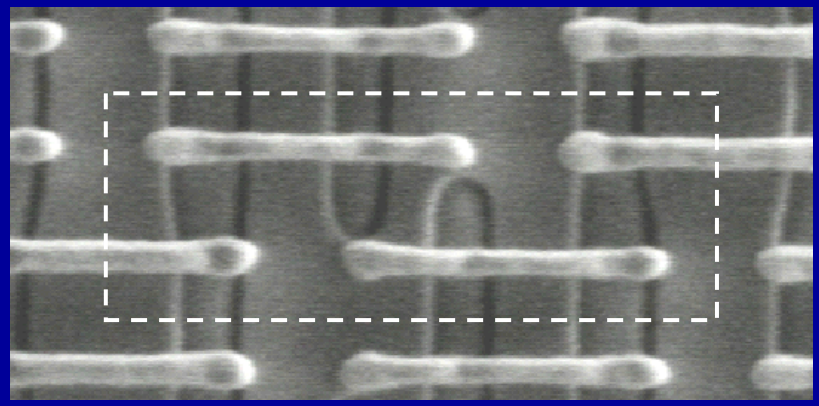
65 nm Generation Interconnects

- Metal 8 layer is added for improved density and performance (1 more layer than 90 nm generation)
- Low-k carbon doped oxide dielectric reduces interconnect capacitance (improved from 90 nm generation)
- Interconnect capacitance is reduced by use of low-k dielectric and by ~0.7x line length scaling
- Lower capacitance improves interconnect performance and reduces chip power

Power Saving Feature



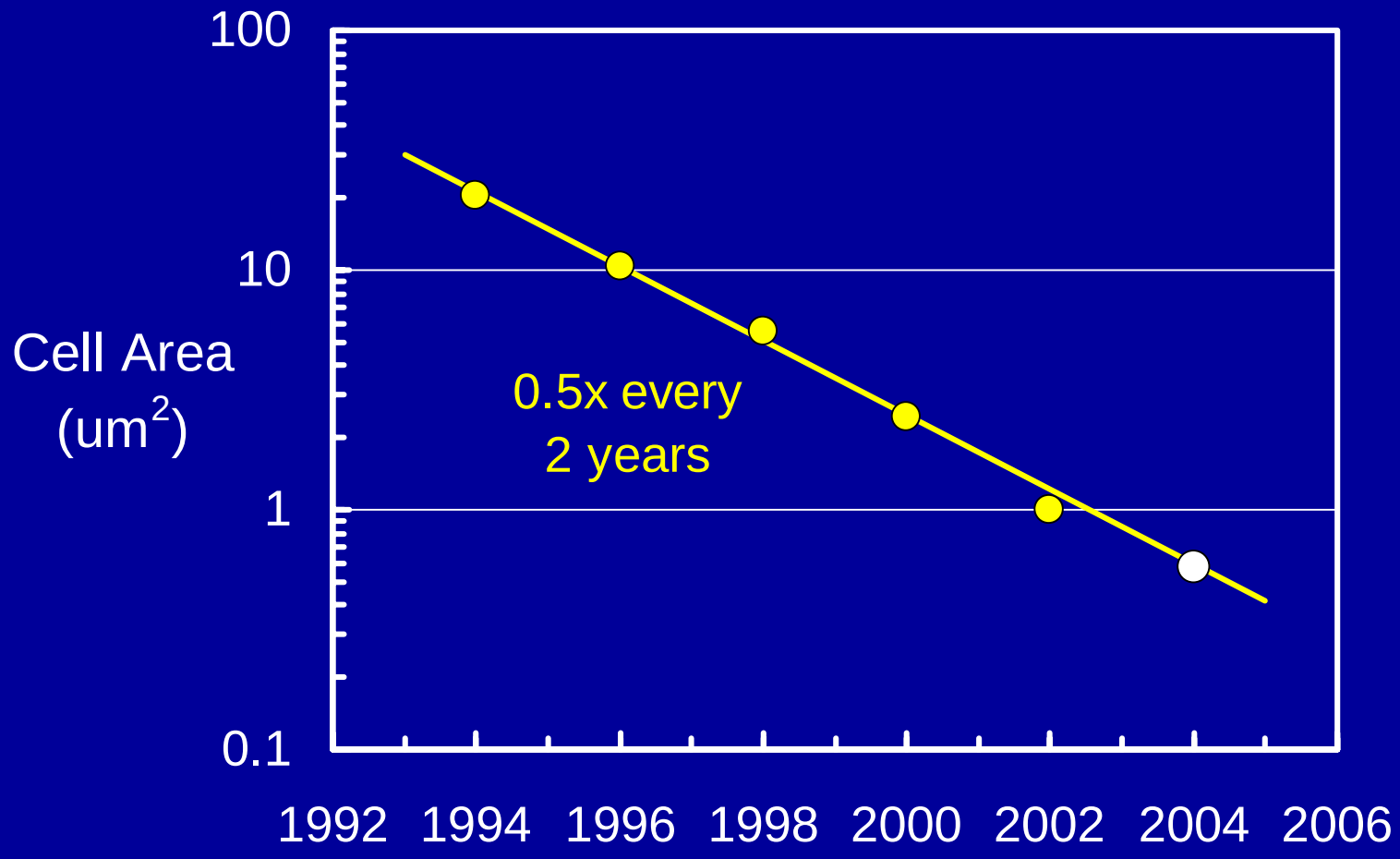
0.57 μm^2 6-T SRAM Cell



- Ultra-small SRAM cell used in 65 nm process packs six transistors in an area of 0.57 μm^2
- Approximately 10 million transistors could fit in the area of the tip of a ball point pen (1 mm^2)
- This SRAM cell is optimized for both small area and ability to operate large arrays at low voltage

Power Saving Feature

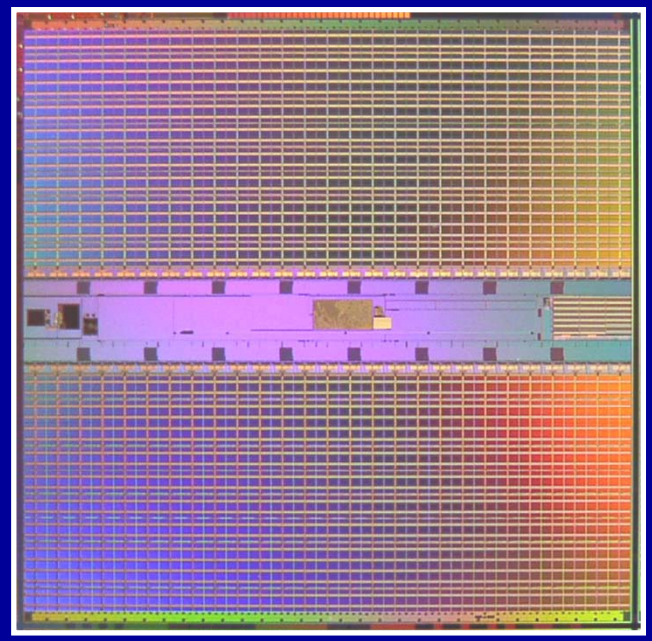
Intel 6-T SRAM Cell Size Trend



Transistor density continues to double every 2 years

70 Mbit SRAM Chip

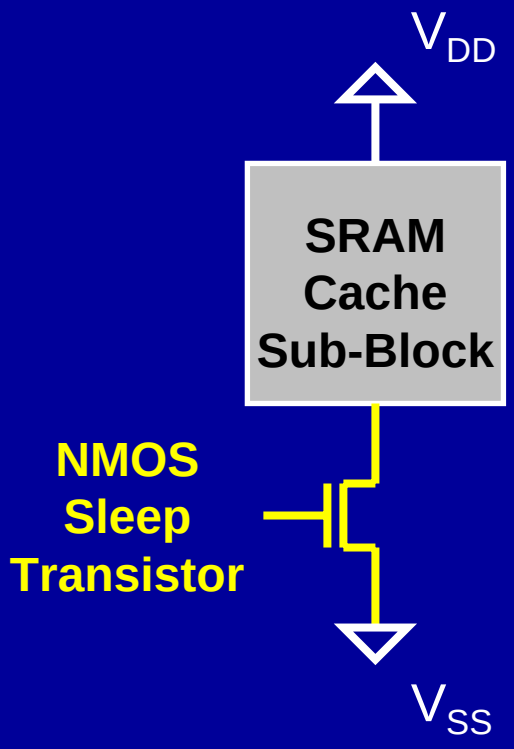
- Fully functional 70 Mbit SRAM chips have been made
- >0.5 billion transistors
- 0.57 μm^2 cell size
- Uses all process features needed for 65 nm logic products



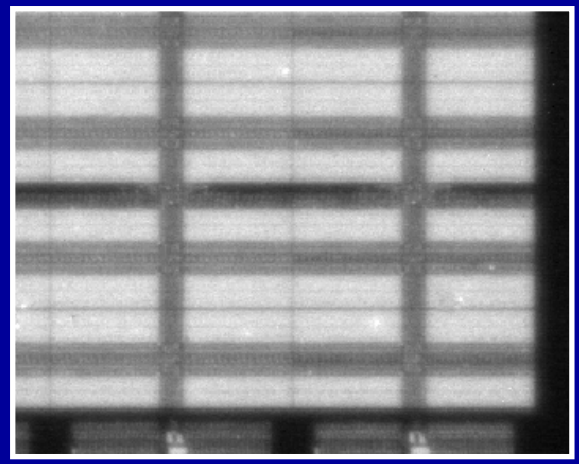
110 mm^2 chip size

No other company has yet demonstrated this level of integration on their 65 nm technology

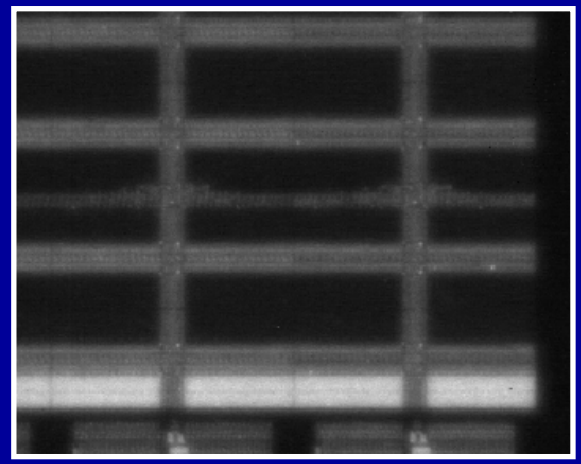
Power Reduction with Sleep Transistors



70 Mbit SRAM IR photos



Normal SRAM block leakage



Sleep transistors shut off leakage in inactive blocks

>3x SRAM leakage reduction with use of sleep transistors

Power Saving Feature

Product Benefits from 65 nm

Intel's 65 nm process technology can:

- Improve CPU performance at constant or lower power by using smaller and faster transistors
- Reduce chip size by a factor of two for previous-generation designs for reduced cost and lower power
- Double the number of transistors per chip at constant chip size
- More transistors add new circuit capabilities and improve CPU performance

65 nm Manufacturing

D1D

- Intel's 65 nm logic technology is being developed at our 300 mm wafer fab, D1D, located in Hillsboro, Oregon
- At 176,000 sq feet, D1D is Intel's largest individual clean room (roughly the size of 3.5 football fields)
- In addition to D1D, the 65 nm process will be manufactured on 300 mm wafers in Fab 12 in Arizona and Fab 24 in Ireland

Summary

- Intel's 65 nm logic technology provides industry-leading density, performance and power reduction features
- With this advanced technology, circuit designers can add more circuit features and increase performance while staying within power limits
- Intel's 65 nm logic technology is being demonstrated on fully functional 70 Mbit SRAM chips with >0.5 billion transistors
- No other company has demonstrated this level of integration on their 65 nm process
- Intel's 65 nm technology is on track for delivery in 2005

More information on Intel's 65 nm logic technology
will be presented in a paper at the

IEEE International Electron Devices Meeting

San Francisco, December 12-15, 2004

For further information on Intel's silicon technology
please visit the Silicon Showcase at

www.intel.com/research/silicon